WHAT IS CLAIMED IS:

1. A circuit comprising:

a first N-type transistor having a first terminal coupled to a power supply, a second terminal and a first gate terminal; and

a filter coupled between the power supply and the first gate terminal.

2. The circuit as recited in claim 1 wherein the filter is configured to reduce noise from the power supply at the first gate terminal.

3. The circuit as recited in claim 1 wherein the filter is a low pass filter.

4. The circuit as recited in claim 3 wherein the low pass filter includes a resistor coupled between the power supply and the first gate terminal and a capacitor coupled between the first gate terminal and ground.

5. The circuit as recited in claim 1 wherein the second terminal is coupled to supply current to a second transistor.

6. The circuit as recited in claim 5 wherein the second transistor includes a third terminal, a fourth terminal, and a second gate terminal, and wherein the third terminal is coupled to the second terminal, and wherein the fourth terminal is an output voltage node.

7. The circuit as recited in claim 6 wherein the second gate terminal is coupled to the output of an operational amplifier circuit, and wherein an output voltage on the output voltage node is a regulated output voltage, and wherein the fourth terminal is coupled to a feedback network which is further coupled to an input of the operational amplifier.

8. The circuit as recited in claim 7 wherein the second gate terminal is coupled to the output of a bandgap generator, and wherein an output voltage on the output voltage node is a reference voltage used as an input to an operational amplifier circuit.

9. A circuit comprising:

a first transistor having a first terminal coupled to a power supply, a second terminal, and a first gate terminal; and

a power control circuit configured, during a time period commencing at power up of the circuit, to supply a voltage to one of the second terminal and the first gate terminal to prevent an overvoltage condition on the first transistor, and wherein the power control circuit is configured, at a termination of the time period, to cease supplying the voltage.

10. The circuit as recited in claim 9 wherein the power control circuit comprises a second transistor having a third terminal, a fourth terminal, and a second gate terminal, and wherein the third terminal is coupled to the power supply, and wherein the fourth terminal is coupled to the one of the second terminal and the first gate terminal, and wherein the power control circuit further comprises a resistor coupled between the power supply and the second gate terminal, and wherein the power control circuit further comprises a capacitor coupled between the second gate terminal and ground.

11. The circuit as recited in claim 10 wherein the second transistor is P-type.

12. The circuit as recited in claim 10 wherein the time period is determined by a time constant corresponding the resistor and the capacitor.

13. The circuit as recited in claim 9 further comprising a resistor coupled between the first gate terminal and the power supply and a capacitor coupled between the first gate terminal and ground.

14. The circuit as recited in claim 13 wherein the power control circuit is coupled to the first gate terminal.

15. The circuit as recited in claim 14 further comprising a second transistor having a third terminal coupled to the power supply, a fourth terminal, and a second gate terminal, and still further comprising a second resistor coupled between the power supply and the second gate terminal and a second capacitor coupled between the second gate terminal and ground, and wherein the power control circuit is coupled to the second gate terminal.

16. A circuit comprising:

an operational amplifier (op amp);

a first transistor having a gate terminal coupled to an output of the op amp and having a first terminal and a second terminal, the first terminal being an output to which a load is couplable, the load being capable of drawing a variable current from the first terminal during operation; and

a first current source coupled to the first terminal, the first current source drawing a first current from the first terminal which is inversely proportional to the current drawn by the load during operation.

17. The circuit as recited in claim 16 wherein the first current source comprises a second transistor, the second transistor being N-type and having a second gate terminal coupled to the output of the op amp, at third terminal coupled to the first terminal, and a fourth

terminal coupled to ground.

18. The circuit as recited in claim 17 wherein the first terminal is coupled to a feedback network which is further coupled as an input to the op amp.

5